

I: INTRODUCTION

The text, *Fundamentals of Logic Design, 7th edition*, has been designed so that it can be used either for a standard lecture course or for a self-paced course. The text is divided into 20 study units in such a way that the average study time for each unit is about the same. The units have undergone extensive class testing in a self-paced environment and have been revised based on student feedback. The study guides and text material are sufficient to allow almost all students to achieve mastery of all of the objectives. For example, the material on Boolean algebra and algebraic simplification is 2½ units because students found this topic difficult. There is a separate unit on going from problem statements to state graphs because this topic is difficult for many students.

The textbook contains answers for all of the problems that are assigned in the study guides. This *Instructor's Manual* contains complete solutions to these problems. Solutions to the remaining homework problems as well as all design and simulation exercises are also included in this manual. In the solutions section of this manual, the abbreviation FLD stands for *Fundamentals of Logic Design* (7th ed.).

Information on the self-paced course as previously taught at the University of Texas using an earlier edition of the textbook is available from Prof. Charles H. Roth, croth@austin.rr.com. In addition to the textbook and study guides, teaching a self-paced course requires that a set of tests be prepared for each study unit. This manual contains a sample test for each unit.

1.1 Using the Text in a Lecture Course

Even though the text was developed in a self-paced environment, the text is well suited for use in a standard lecture course. Since the format of the text differs somewhat from a conventional text, a few suggestions for using the text in a lecture course may be appropriate. Except for the inclusion of objectives and study guides, the units in the text differ very little from chapters in a standard textbook. The study guides contain very basic questions, while the problems at the end of each unit are of a more comprehensive nature. For this reason, we suggest that specific study guide questions be assigned for students to work through on their own before working out homework problems selected from those at the end of the unit. The unit tests given in Part IV of this manual provide a convenient source of additional homework assignments or a source of quiz problems. The text contains many examples that are completely worked out with detailed step-by-step explanations. Discussion of these detailed examples in lecture may not be necessary if the students study them on their own. The lecture time is probably better spent discussing general principles and applications as well as providing help with some of the more difficult topics. Since all of the units have study guides, it would be possible to assign some of the easier topics for self-study and devote the lectures to the more difficult topics.

At the University of Texas a class composed largely of Electrical Engineering and Computer Science sophomores and juniors covers 18 units (all units except 6 and 19) of the text in one semester. Units 8, 10, 12, 16, 17, and 20 contain design problems that are suitable for simulation and lab exercises. The design problems help tie together and review the material from a number of preceding units. Units 10, 17, and 20 introduce the VHDL

hardware description language. These units may be omitted if desired since no other units depend on them.

1.2 Some Remarks About the Text

In this text, students are taught how to use Boolean algebra effectively, in contrast with many texts that present Boolean algebra and a few examples of its application and then leave it to the student to figure out how to use it effectively. For example, use of the theorem $x + yz = (x + y)(x + z)$ in factoring and multiplying out expressions is taught explicitly, and detailed guidelines are given for algebraic simplification.

Sequential circuits are given proper emphasis, with over half of the text devoted to this subject. The pedagogical strategy the text uses in teaching sequential circuits has proven to be very effective. The concepts of state, next state, etc. are first introduced for individual flip-flops, next for counters, then for sequential circuits with inputs, and finally for more abstract sequential circuit models. The use of timing charts, a subject neglected by many texts, is taught both because it is a practical tool widely used by logic design engineers and because it aids in the understanding of sequential circuit behavior.

The most important and often most difficult part of sequential circuit design is formulating the state table or graph from the problem statement, but most texts devote only a few paragraphs to this subject because there is no algorithm. This text devotes a full unit to the subject, presents guidelines for deriving state tables and graphs, and provides programmed exercises that help the student learn this material. Most of the material in the text is treated in a fairly conventional manner with the following exceptions:

- (1) The diagonal form of the 5-variable Karnaugh map is introduced in Unit 5. (We find that students make fewer mistakes when using the diagonal form of 5-variable map in comparison with the side-by-side form.) Unit 5 also presents a simple algorithm for finding all essential prime implicants from a Karnaugh map.
- (2) Both the state graph approach (Unit 18) and the SM chart approach (Unit 19) for designing sequential control circuits are presented.
- (3) The introduction to the VHDL hardware description language in Units 10, 17, and 20 emphasizes the relation between the VHDL code and the actual hardware.

1.3 Using the Text in a Self-Paced Course

This section introduces the personalized system of self-paced instruction (PSI) and offers suggestions for using the text in a self-paced course. PSI (Personalized System of Instruction) is one of the most popular and successful systems used for self-paced instruction. The essential features of the PSI method are

- (a) Students are permitted to pace themselves through the course at a rate commensurate with their ability and available time.
- (b) A student must demonstrate mastery of each study unit before going onto the next.
- (c) The written word is stressed; lectures, if used, are only for motivation and not for transmission of critical information.
- (d) Use of proctors permits repeated testing, immediate scoring, and significant personal interaction with the students.

These factors work together to motivate students toward a high level of achievement in a well-

designed PSI course.

The PSI method of instruction and its implementation are described in detail in the following references:

1. Keller, Fred S. and J. Gilmour Sherman, *The Keller Plan Handbook*, W. A. Benjamin, Inc., 1974.
2. Sherman, J.G., ed., *Personalized System of Instruction: 41 Germinal Papers*, W. A. Benjamin, Inc., 1974.
3. Roth, C. H., *The Personalized System of Instruction – 1962 to 1998*, presented at the 1999 ASEE Annual Conference. (Go to <http://search.asee.org> and search under Conference Papers for “The Personalized System of Instruction”.)

Results of applying PSI to a first course in logic design of digital systems are described in Roth, C.H., *Continuing Effectiveness of Personalized Self-Paced Instruction in Digital Systems Engineering*, Engineering Education, Vol. 63, No. 6, March 1973.

The instructor in charge of a self-paced course will serve as course manager in addition to his role in the classroom. For a small class, he may spend a good part of his time acting as proctor in the classroom, but as class size increases he will have to devote more of his time to supervision of course activities and less time to individual interaction with students. In his managerial role, the instructor is responsible for organizing the course, selection and training of proctors, supervision of proctors, and monitoring of student progress. The proctors play an important role in the success of a self-paced course, and therefore their selection, training, and supervision is very important. After an initial session to discuss proper ways of grading readiness tests and interacting with students, weekly proctor meetings to discuss course procedures and problems may be appropriate.

A progress chart showing the units completed by each student is very helpful in monitoring student progress through the course. The instructor may wish to have individual conferences with students who fall too far behind. The instructor needs to be available in the classroom to answer individual student questions and to assist with grading of readiness tests as needed. He should make a special point to speak with the weak or slow students and give them a word of encouragement. From time to time he may need to settle differences which arise between proctors and students.

Various strategies for organizing a PSI course are described in the *Keller Plan Handbook*. The procedures previously used for operating the self-paced digital logic course at the University of Texas are described in “Unit 0”, which is available from Prof. Charles H. Roth, croth@austin.rr.com. At the first class meeting, we handed out a copy of Unit 0. The students were asked to read through Unit 0 and take a short test on the course procedures. This test was immediately evaluated so that the student could complete Unit 0 before the end of the first class period. In this way, the student was exposed to the basic way the course operated and was ready to proceed immediately with Unit 1 in the textbook.

During a typical class period, some of the students spent their time studying but most of the students came prepared to take a unit test. At the beginning of the period, the instructor or a proctor was available to answer student questions on an individual basis. Later in the

period, most of the time was spent evaluating unit tests. We found that a standard 50 minute class period was not long enough for a PSI session. We usually scheduled sessions of 1½ or 2 hours or longer depending on class size. This allowed adequate time for students to have their questions answered, take a unit test, and have their tests graded. Interactive grading of the tests with the student present is an important part of the PSI system and adequate time must be allowed for this activity. If you have a large number of students and proctors, you may wish to prepare a manual for guidance of your proctors. The procedures that we used for evaluating unit tests are described in a Proctor's Manual, which can be obtained by writing to Professor Charles H. Roth.

1.4. Use of Computer Software

Three software packages are included on the CD that accompanies the textbook. The first is a logic simulator program called *SimUaid*, the second is a basic computer-aided logic design program called *LogicAid*, and the third is a VHDL Simulator called *DirectVHDL*. In addition, we use the Xilinx ISE software for synthesizing VHDL code and downloading to CPLD or FPGA circuit boards. The Xilinx ISE software is available at nominal cost through the Xilinx University Program (for information, go to www.xilinx.com/university/index.htm). A “Webpack” version of the Xilinx software is also available for downloading from the Xilinx.com website.

SimUaid provides an easy way for students to test their logic designs by simulating them. We first introduce *SimUaid* in Unit 4, where we ask the students to design a simple logic circuit such as problem 4.13 or 4.14, and simulate it. *SimUaid* is easy to learn, and it is highly interactive so that students can flip a simulated switch and immediately observe the result. In Unit 8, students design a multiple-output combinational logic circuit using NAND and NOR gates and test its operation using *SimUaid*. Students can use the simulator to help them understand the operation of latches and flip-flops in Unit 11. In Unit 12, we ask them to design a counter and simulate it (one part of problem 12.10). In Unit 16, students use *SimUaid* to test their sequential circuit designs. They can also generate VHDL code from their *SimUaid* circuit, synthesize it, and download it to a circuit board for hardware testing. In Unit 18, students can use the advanced features of *SimUaid* to simulate a multiplier or divider controlled by a state machine.

LogicAid provides an easy way to introduce students to the use of the computer in the logic design process. It enables them to solve larger, more practical design problems than they could by hand. They can also use *LogicAid* to verify solutions that they have worked out by hand. Instructors can use the program for grading homework and quizzes. We first introduce *LogicAid* in Unit 5. The program has a Karnaugh Map Tutorial mode that is very useful in teaching students to solve Karnaugh map problems. This tutorial mode helps students learn to derive minimum solutions from a Karnaugh map by informing them at each step whether that step is correct or not. It also forces them to choose essential prime implicants first. When in the KMap tutor mode, *LogicAid* prints “KMT” at the top of each output page, so you can check to see if the problems were actually solved in the tutorial mode.

Students can use *LogicAid* to help them solve design problems in Units 8, 16, 18, 19 and other units. For designing sequential circuits, they can input a state graph, convert it to a state table, reduce the state table, make a state assignment, and derive minimized logic equations for outputs and flip-flop inputs.

The *LogicAid* State Table Checker is useful for Units 14 and 16, and for other units in which students construct state tables. It allows students to check their solutions without revealing the correct

answers. If the solution is wrong, the program displays a short input sequence for which the student's table fails. The *LogicAid* folder on the CD contains encoded copies of solutions for most of the state graph problems in *Fundamentals of Logic Design, 7th Ed.* If you wish to create a password-protected solution file for other state table problems, enter the state table into *LogicAid*, syntax check it, and then hold down the Ctrl key while you select Save As on the file menu. The Partial Graph Checker serves as a state graph tutor that allows a student to check his work at each step while constructing a state graph. If the student makes a mistake, it provides feedback so that the student can correct his answer. The partial graph checker works with any state graph problem for which an encoded state table solution file is provided.

The DirectVHDL simulator helps students learn VHDL syntax because it provides immediate visual feedback when they make mistakes. Our students use it for simulating VHDL code in Units 10, 17, and 20. Students can simulate and debug their code at home and then bring the code into lab for synthesis and hardware testing.

1.5. Suggested Equipment for Laboratory Exercises

Many types of logic lab equipment are available that are adequate to perform the lab exercises. Since most logic design is done today using programmable logic instead of individual ICs, we now recommend use of CPLDs or FPGAs for hardware implementation of logic circuit designs. At the University of Texas, we are presently using the XILINX Spartan-3 FPGA boards, which are available from Digilent. The Spartan-3 FPGA has more than an adequate number of logic cells to implement the lab exercises in the text. The board has 8 switches, 4 pushbuttons, 8 single LEDs, and four 7-segment LEDs.. Information about this board and other CPLD and FPGA boards made by Digilent can be found on their website, www.digilentinc.com. We use the board in conjunction with the Xiliinx ISE software mentioned earlier.

Unit 1 Solutions

1.13 $544.1_9 = 5 \times 9^2 + 4 \times 9^1 + 4 \times 9^0 + 1 \times 9^{-1}$
 $= 5 \times 81 + 4 \times 9 + 4 + 1/9$
 $= 445 \frac{1}{9}_{10}$

$$\begin{array}{r|l} 16 \overline{)445} & 1/9 \\ 16 \overline{)27} & r13 \quad \underline{16} \\ 16 \overline{)1} & r11 \quad (1)7/9 \\ \underline{0} & r1 \quad \underline{16} \\ & (12)4/9 \\ & \underline{16} \\ & (7)1/9 \end{array}$$

$\therefore 544.1_9 = 1BD.1C7_{16}$
 $= 1\ 1011\ 1101.0001\ 1100\ 0111_2...$

1.14 (d)

$$\begin{array}{r|l} 3 \overline{)97} & .7 \\ 3 \overline{)32} & r1 \quad \underline{3} \\ 3 \overline{)10} & r2 \quad (2).1 \\ 3 \overline{)3} & r1 \quad \underline{3} \\ 3 \overline{)1} & r0 \quad \underline{(0).3} \\ \underline{0} & r1 \quad 3 \\ & \underline{(0).9} \\ & 3 \\ & (2).7 \end{array}$$

$\therefore 97.7_{10} = 10121.2002..._3$

1.14 (e)

$$\begin{array}{r|l} 5 \overline{)97} & .7 \\ 5 \overline{)19} & r2 \quad \underline{5} \\ 5 \overline{)3} & r4 \quad (3).5 \\ \underline{0} & r3 \quad \underline{5} \\ & \underline{(2).5} \end{array}$$

$\therefore 97.7_{10} = 342.322..._5$

1.16 (a) $2983\ 63/64_{10} =$

$$\begin{array}{r|l} 8 \overline{)2983} & 0.984 \\ 8 \overline{)372} & r7 \quad \underline{8} \\ 8 \overline{)46} & r4 \quad (7).872 \\ 9 \overline{)5} & r6 \quad \underline{8} \\ \underline{0} & r5 \quad (6).976 \end{array}$$

$\therefore 2983\ 63/64_{10} = 5647.76_8$ (or 5647.77_8)
 $= 101\ 110\ 100\ 111.111\ 110_2$
(or $101\ 110\ 100\ 111.111\ 111_2$)

1.16 (c) $1900\ 31/32_{10}$

$$\begin{array}{r|l} 8 \overline{)1900} & 0.969 \\ 8 \overline{)273} & r4 \quad \underline{8} \\ 8 \overline{)29} & r5 \quad (7).752 \\ 9 \overline{)3} & r5 \quad \underline{8} \\ \underline{0} & r3 \quad (6).016 \end{array}$$

$\therefore 1900\ 31/32_{10} = 3554.76_8$
 $= 011\ 101\ 101\ 100.111\ 110_2$

1.14 (a), (c)

$$\begin{array}{r|l} 16 \overline{)97} & .7 \\ 16 \overline{)6} & r1 \quad \underline{16} \\ \underline{0} & r6 \quad (11).2 \\ & \underline{16} \\ & (3).2 \end{array}$$

$\therefore 97.7_{10} = 61.B3333..._{16}$

(a) $61.B3333..._{16}$

$= 110\ 0001.1011\ 0011\ 0011\ 0011..._2$

(b) $1\ 100\ 001.101\ 100\ 110\ 011\ 001\ 100\ 11..._2$

$= 141.5\ 4631\ 4631..._8$

1.15

1110212.20211_3
 $01\ 11\ 02\ 12.20\ 21\ 10 = 1425.673_9$

| Base 3 | Base 9 |
|--------|--------|
| 00 | 0 |
| 01 | 1 |
| 02 | 2 |
| 10 | 3 |
| 11 | 4 |
| 12 | 5 |
| 20 | 6 |
| 21 | 7 |
| 22 | 8 |

1.16 (b)

$$\begin{array}{r|l} 93.70_{10} & \\ 8 \overline{)93} & 0.70 \\ 8 \overline{)11} & r5 \quad \underline{8} \\ 8 \overline{)1} & r3 \quad (5).60 \\ \underline{0} & r1 \quad \underline{8} \\ & (4).80 \end{array}$$

$\therefore 93.70_{10} = 135.54_8 = 001\ 011\ 101.101\ 100_2$

1.16 (d)

$$\begin{array}{r|l} 109.30_{10} & 0.30 \\ 8 \overline{)109} & 0.30 \\ 8 \overline{)13} & r5 \quad \underline{8} \\ 8 \overline{)1} & r5 \quad (2).40 \\ \underline{0} & r1 \quad \underline{8} \\ & (3).20 \end{array}$$

$\therefore 109.30_{10} = 155.23_8$
 $= 001\ 101\ 101.010\ 011_2$

Unit 1 Solutions

1.17 (a)

$$\begin{array}{r} \overset{1}{1}111 \text{ (Add)} \\ \underline{1001} \\ 11000 \end{array} \quad \begin{array}{r} \overset{1}{1}111 \text{ (Subtract)} \\ \underline{1001} \\ 0110 \end{array}$$

$$\begin{array}{r} 1111 \text{ (Multiply)} \\ \underline{1001} \\ 1111 \\ \underline{0000} \\ 01111 \\ \underline{0000} \\ 001111 \\ \underline{1111} \\ 10000111 \end{array}$$

1.17 (b)

$$\begin{array}{r} \overset{1}{1}101001 \text{ (Add)} \\ \underline{110110} \\ 10011111 \end{array} \quad \begin{array}{r} \overset{1}{1}101001 \text{ (Sub)} \\ \underline{110110} \\ 110011 \end{array}$$

$$\begin{array}{r} 1101001 \text{ (Mult)} \\ \underline{110110} \\ 0000000 \\ \underline{1101001} \\ 11010010 \\ \underline{1101001} \\ 1001110110 \\ \underline{0000000} \\ 1001110110 \\ \underline{1101001} \\ 100100000110 \\ \underline{1101001} \\ 1011000100110 \end{array}$$

1.17(c)

$$\begin{array}{r} \overset{1}{1}10010 \text{ (Add)} \\ \underline{11101} \\ 1001111 \end{array} \quad \begin{array}{r} \overset{1}{1}10010 \text{ (Sub)} \\ \underline{11101} \\ 10101 \end{array}$$

$$\begin{array}{r} 110010 \text{ (Mult)} \\ \underline{11101} \\ 110010 \\ \underline{000000} \\ 0110010 \\ \underline{110010} \\ 11111010 \\ \underline{110010} \\ 1010001010 \\ \underline{110010} \\ 10110101010 \end{array}$$

1.18

$$\text{(a)} \quad \begin{array}{r} \overset{1}{1}0100100 \\ \underline{01110011} \\ 0110001 \end{array} \quad \text{(b)} \quad \begin{array}{r} \overset{1}{1}0010011 \\ \underline{01011001} \\ 00111010 \end{array}$$

$$\text{(c)} \quad \begin{array}{r} \overset{1}{1}1110011 \\ \underline{10011110} \\ 01010101 \end{array}$$

1.19(a)

$$\begin{array}{r} 101110 \text{ Quotient} \\ 101 \overline{)11101001} \\ \underline{101} \\ 1001 \\ \underline{101} \\ 1000 \\ \underline{101} \\ 110 \\ \underline{101} \\ 11 \text{ Remainder} \end{array}$$

1.19(b)

$$\begin{array}{r} 11011 \text{ Quotient} \\ 1110 \overline{)110000001} \\ \underline{1110} \\ 10100 \\ \underline{1110} \\ 11000 \\ \underline{1110} \\ 10101 \\ \underline{1110} \\ 111 \text{ Remainder} \end{array}$$

1.19(c)

$$\begin{array}{r} 1100 \text{ Quotient} \\ 1001 \overline{)1110010} \\ \underline{1001} \\ 1010 \\ \underline{1001} \\ 110 \text{ Remainder} \end{array}$$

1.20(a)

$$\begin{array}{r} 10111 \text{ Quotient} \\ 110 \overline{)10001101} \\ \underline{110} \\ 1011 \\ \underline{110} \\ 1010 \\ \underline{110} \\ 1001 \\ \underline{110} \\ 11 \text{ Remainder} \end{array}$$

Unit 1 Solutions

1.20(b)

$$\begin{array}{r}
 \overline{)100011} \text{ Quotient} \\
 1011 \overline{)110000011} \\
 \underline{1011} \\
 10001 \\
 \underline{1011} \\
 1101 \\
 \underline{1011} \\
 10 \text{ Remainder}
 \end{array}$$

1.20(c)

$$\begin{array}{r}
 \overline{)1011} \text{ Quotient} \\
 1010 \overline{)1110100} \\
 \underline{1010} \\
 10010 \\
 \underline{1010} \\
 10000 \\
 \underline{1010} \\
 110 \text{ Remainder}
 \end{array}$$

1.21 (a) $4 + 3$ is 10 in base 7, i.e., the sum digit is 0 with a carry of 1 to the next column. $1 + 5 + 4$ is 10 in base 7. $1 + 6 + 0$ is 10 in base 7. This overflows since the correct sum is 1000_7 .

(b) $4 + 3 + 3 + 3 = 13$ in base 10 and 23 in base 5. Try base 10. $1 + 2 + 4 + 1 + 3 = 11$ in base 10 so base 10 does not produce a sum digit of 2. Try base 5. $2 + 2 + 4 + 1 + 3 = 22$ in base 5 so base 5 works.

(c) $4 + 3 + 3 + 3 = 31$ in base 4, 21 in base 6, and 11 in base 12. Try base 12. $1 + 2 + 4 + 1 + 3 = B$ in base 12 so base 12 does not work. Try base 4. $3 + 2 + 4 + 1 + 3 = 31$ in base 4 so base 4 does not work. Try base 6. $2 + 2 + 4 + 1 + 3 = 20$ so base 6 is correct.

1.24 (a) Expand the base b number into a power series

$N = d_{3k-1}b^{3k-1} + d_{3k-2}b^{3k-2} + d_{3k-3}b^{3k-3} + \dots + d_5b^5 + d_4b^4 + d_3b^3 + d_2b^2 + d_1b^1 + d_0b^0 + d_{-1}b^{-1} + d_{-2}b^{-2} + d_{-3}b^{-3} + \dots + d_{-3m+2}b^{-3m+2} + d_{-3m+1}b^{-3m+1} + d_{-3m}b^{-3m}$ where each d_i has a value from 0 to $(b-1)$. (Note that 0's can be appended to the number so that it has a multiple of 3 digits to the left and right of the radix point.) Factor b^3 from each group of 3 consecutive digits of the number to obtain

$$\begin{aligned}
 N &= (d_{3k-1}b^2 + d_{3k-2}b^1 + d_{3k-3}b^0)(b^3)^{(k-1)} + \dots \\
 &+ (d_5b^2 + d_4b^1 + d_3b^0)(b^3)^1 + (d_2b^2 + d_1b^1 + d_0b^0)(b^3)^0 + (d_{-1}b^2 + d_{-2}b^1 + d_{-3}b^0)(b^3)^{-1} + \dots + \\
 &(d_{-3m+2}b^2 + d_{-3m+1}b^1 + d_{-3m}b^0)(b^3)^{-m}
 \end{aligned}$$

Each $(d_{3i-1}b^2 + d_{3i-2}b^1 + d_{3i-3}b^0)$ has a value from 0 to $[(b-1)b^2 + (b-1)b^1 + (b-1)b^0]$

$$= (b-1)(b^2 + b^1 + b^0) = (b^3 - 1)$$

so it is a valid digit in a base b^3 number.

Consequently, the last expression is the power series expansion for a base b^3 number.

1.25(a) $(5 - 1) = 4_5$, $(5^2 - 1) = 44_5$ and $(5^3 - 1) = 444_5$

1.25(b)

$$\begin{aligned}
 (b^n - 1) &= (b - 1)(b^{n-1}) + b^{n-1} \\
 &= (b - 1)b^{n-1} + (b - 1)b^{n-2} + b^{n-2} \\
 &= (b - 1)b^{n-1} + (b - 1)b^{n-2} + \dots \\
 &\quad + (b - 1)b + (b - 1)
 \end{aligned}$$

This expression is the polynomial expansion for the base b number with n digits $(b - 1)(b - 1) \dots (b - 1)$

1.22 If the binary number has n bits (to the right of the radix point), then its precision is $(1/2^{n+1})$. So to have the same precision, n must satisfy

$$(1/2^{n+1}) < (1/2)(1/10^4) \text{ or } n > 4/(\log 2) = 13.28 \text{ so } n \text{ must be } 14.$$

1.23

$$\begin{aligned}
 &.363636\dots \\
 &= (36/10^2)(1 + 1/10^2 + 1/10^4 + 1/10^6 + \dots) \\
 &= (36/10^2)[1/(1 - 1/10^2)] = (36/10^2)[10^2/99] \\
 &= 36/99 = 4/11
 \end{aligned}$$

$$8(4/11) = 2 + 10/11$$

$$8(10/11) = 7 + 3/11$$

$$8(3/11) = 2 + 2/11$$

$$8(2/11) = 1 + 5/11$$

$$8(5/11) = 3 + 7/11$$

$$8(7/11) = 5 + 1/11$$

$$8(1/11) = 0 + 8/11$$

$$8(8/11) = 5 + 9/11$$

$$8(9/11) = 6 + 6/11$$

$$8(6/11) = 4 + 4/11$$

$$8(4/11) = 2 + 10/11$$

Repeats: .27213505642.....

1.24 (b) Expand the base b^3 number into a power series

$$N = d_k(b^3)^k + d_{k-1}(b^3)^{k-1} + \dots + d_1(b^3)^1 + d_0(b^3)^0 + d_{-1}(b^3)^{-1} + \dots + d_{-m}(b^3)^{-m}$$

where each d_i has a value from 0 to $(b^3 - 1)$. Consequently, d_i can be represented as a base b number in the form

$$(e_{3i-1}b^2 + e_{3i-2}b^1 + e_{3i-3}b^0)$$

Where each e_j has a value from 0 to $(b-1)$.

Substituting these expressions for the d_i produces a power series expansion for a base b number.

1.26(a) $(b + 1)^2 = b^2 + 2b + 1$ so $(11_b)^2 = 121_b$ if $b > 2$.

1.26(b) $(b^2 + b + 1)^2 = b^4 + 2b^3 + 3b^2 + 2b + 1$ so $(111_b)^2 = 12321_b$ if $b > 3$.

1.26(c) $(b^2 + 2b + 1)^2 = b^4 + 4b^3 + 6b^2 + 4b + 1$ so $(121_b)^2 = 14641_b$ if $b > 6$.

1.26(d) $(b^3 + b^2 + b + 1)^2 = b^6 + 2b^5 + 3b^4 + 4b^3 + 3b^2 + 2b + 1$ so $(1111_b)^2 = 1234321_b$ if $b > 4$.

Unit 1 Solutions

1.27(a) $(0.12)_3 = (1/3 + 2/9)_{10} = (2/6 + 8/36)_{10}$
 $= (3/6 + 2/36)_{10} = (0.32)_6$

1.27(b) $(0.375)_{10} = (3/8)_{10} = (0.3)_8$

1.27(c) $(a_{-1}R^{-1} + a_{-2}R^{-2} + \dots + a_{-m}R^{-m})S^n$ will be an integer for every N only if R^m divides S^n for some n. Hence, each factor of R must be a factor of S, not necessarily the same number of times.

1.27(d) For a specific number N, $(a_{-1}R^{-1} + a_{-2}R^{-2} + \dots + a_{-m}R^{-m})S^n$ will be an integer if each factor of R^m is a factor of either S^n or $(a_{-1}R^{m-1} + a_{-2}R^{m-2} + \dots + a_{-m})$

1.30 5-4-1-1 is not possible, because there is no way to represent 3 or 8. 6-3-2-1 is possible:

| | |
|---|---------|
| | 6 3 2 1 |
| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 0 |
| 3 | 0 1 0 0 |
| 4 | 0 1 0 1 |
| 5 | 0 1 1 0 |
| 6 | 1 0 0 0 |
| 7 | 1 0 0 1 |
| 8 | 1 0 1 0 |
| 9 | 1 1 0 0 |

1.33

Alternate Solutions:

| | |
|---|---------|
| | 7 3 2 1 |
| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 0 |
| 3 | 0 1 0 0 |
| 4 | 0 1 0 1 |
| 5 | 0 1 1 0 |
| 6 | 0 1 1 1 |
| 7 | 1 0 0 0 |
| 8 | 1 0 0 1 |
| 9 | 1 0 1 0 |
| A | 1 1 0 0 |
| B | 1 1 0 1 |

$B4A9 = 1101\ 0101\ 1100\ 1010$
 Alt.: = " " 1011 "

1.28

| | |
|---|---------|
| | 4 3 2 1 |
| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 0 |
| 3 | 0 1 0 0 |
| 4 | 1 0 0 0 |
| 5 | 1 0 0 1 |
| 6 | 1 0 1 0 |
| 7 | 1 1 0 0 |
| 8 | 1 1 0 1 |
| 9 | 1 1 1 0 |

$9154 = 1110\ 0001\ 1001\ 1000$

1.29

5-3-1-1 is possible, but 6-4-1-1 is not, because there is no way to represent 3 or 9.

Alternate Solutions:

| | |
|---|---------|
| | 5 3 1 1 |
| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 1 |
| 3 | 0 1 0 0 |
| 4 | 0 1 0 1 |
| 5 | 1 0 0 0 |
| 6 | 1 0 0 1 |
| 7 | 1 0 1 1 |
| 8 | 1 1 0 0 |
| 9 | 1 1 0 1 |

1.31

Alternate Solutions:

Alternate Solutions:

| | |
|---|---------|
| | 6 2 2 1 |
| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 0 |
| 3 | 0 0 1 1 |
| 4 | 0 1 1 0 |
| 5 | 0 1 1 1 |
| 6 | 1 0 0 0 |
| 7 | 1 0 0 1 |
| 8 | 1 0 1 0 |
| 9 | 1 0 1 1 |

$1100\ 0011 = 83$

$1110\ 0110 = 94$

1.34

(a)

| | |
|---|---------|
| | 8 4-2-1 |
| 0 | 0 0 0 0 |
| 1 | 0 1 1 1 |
| 2 | 0 1 1 0 |
| 3 | 0 1 0 1 |
| 4 | 0 1 0 0 |
| 5 | 1 0 1 1 |
| 6 | 1 0 1 0 |
| 7 | 1 0 0 1 |
| 8 | 1 0 0 0 |
| 9 | 1 1 1 1 |

(b) The 9's complement of a decimal number represented with this weighted code can be obtained by replacing 0's with 1's and 1's with 0's (bit-by-bit complement).

Unit 1 Solutions

1.38 (c)

| | |
|--------------------------|--|
| <u>In 2's complement</u> | <u>In 1's complement</u> |
| 10001 | 10001 |
| + 10110 | + 10101 |
| (1)00111 | (1)00110 |
| <i>overflow</i> | $\begin{array}{c} \text{---} \rightarrow 1 \\ \text{00111} \\ \text{overflow} \end{array}$ |

1.38 (d)

| | |
|--------------------------|--------------------------|
| <u>In 2's complement</u> | <u>In 1's complement</u> |
| 10101 | 10101 |
| + 00110 | + 00101 |
| 11011 | 11010 |

1.39 (a)

| | |
|--|-----------------|
| <u>add</u> | <u>subt</u> |
| 101010 | 101010 |
| + 011101 | - 011101 |
| (1)000111 | 001101 |
| $\begin{array}{c} \text{---} \rightarrow 1 \\ \text{001000} \end{array}$ | <i>overflow</i> |

1.40 (a)

| | |
|---------------------|-------------------|
| | <u>complement</u> |
| i) 00000000 (0) | 11111111 (-0) |
| ii) 11111110 (-1) | 00000001 (1) |
| iii) 00110011 (51) | 11001100 (-51) |
| iv) 10000000 (-127) | 01111111 (127) |

(b)

| | |
|------------|-----------------|
| <u>add</u> | <u>subt</u> |
| 101010 | 101010 |
| + 011101 | - 011101 |
| (1)000111 | 001101 |
| | <i>overflow</i> |

(b)

| | |
|---------------------|-----------------|
| i) 00000000 (0) | 00000000 (0) |
| ii) 11111110 (-2) | 00000010 (2) |
| iii) 00110011 (51) | 11001101 (-51) |
| iv) 10000000 (-128) | 10000000 (-128) |

1.41 (a) (16)(4) = 64, add 2 0's to get 6400
 (10)(2) = 20, add 1 0 to get 200
 (7)(1) = 7
 6400 + 200 + 7 = 6607

1.42 (a) If $A + B \leq 2^{n-1} - 1$, then the sign bit of $A + B$ is 0 indicating a positive number with magnitude $A + B$. If $A + B > 2^{n-1} - 1$, then the sign bit of $A + B$ is 1 indicating a negative number with magnitude $2^n - (A + B)$.

(b) $(d_{n-1}d_{n-2} \dots d_1d_0)_2 = d_{n-1}(20)^{n-1} + d_{n-2}(20)^{n-2} + \dots + d_1(20)^1 + d_0(20)^0 = d_{n-1}(2)^{n-1}(10)^{n-1} + d_{n-2}(2)^{n-2}(10)^{n-2} + \dots + d_1(2)^1(10)^1 + d_0(2)^0(10)^0 =$ The general term in the expansion is $d_i(2)^i(10)^i$. The multiplication by $(10)^i$ adds i 0's on the right of $d_i(2)^i$.

(b) If $A \geq B$, then $A + (-B) = A + (2^n - B) = 2^n + (A - B)$ is $\geq 2^n$ so there is a carry from the sign position that is ignored and the sum is $(A - B)$. If $A < B$, then $A + (-B) = A + (2^n - B) = 2^n - (B - A)$ is $< 2^n$ and $> 2^{n-1}$ so there is no carry from the sign position and the sign bit is 1. $2^n - (B - A)$ represents a negative number of magnitude $(B - A)$.

(c) The algorithm would be divide d_i by 2^i and shift the result i places to the right, then add all terms.

(c) After ignoring the carry from the sign position, $(2^n - A) + (2^n - B) = 2^n - (A + B)$. If $(A + B) \leq 2^{n-1}$, $2^n - (A + B) \geq 2^n - 2^{n-1} = 2^{n-1}$ so the sign bit of $2^n - (A + B)$ is 1 indicating a negative number with magnitude $(A + B)$. If $(A + B) > 2^{n-1}$, $2^n - (A + B) < 2^n - 2^{n-1} = 2^{n-1}$ so the sign bit of $2^n - (A + B)$ is 0 indicating a positive number with magnitude $2^n - (A + B)$.

(d) $15/2 = 7.5$ shifted right 1 place is 0.75
 $10/4 = 2.5$ shifted right 2 places is 0.025
 $7/8 = 0.875$ shifted right 3 places is 0.000875
 $0.75 + 0.025 + 0.000875 = 0.775875$

1.43 A and B positive: Overflow does not occur if $A + B \leq 2^n - 1 - 1$ in which case $A + B$ has a sign bit of 0 and has a magnitude of $A + B$.
 A positive and B negative and $A > |B|$: $A + 2^n - 1 - B = 2^n - 1 + (A - B) > 2^n - 1$ so there is a carry from the sign position and, after the end-around carry, the result is $(A - B)$.
 A positive and B negative and $A \leq |B|$: $A + 2^n - 1 - B = 2^n - 1 - (B - A) \leq 2^n - 1$ so there is no carry from the sign position and the sign bit is 1 so the result represents a negative number with magnitude $(B - A)$.

1.43 cont. A and B negative: $(2^n - 1 - A) + (2^n - 1 - B) = 2^n - 1 - (A + B)$ after the end-around carry. There is no overflow if $A + B \leq 2^n - 1 - 1$ in which case $2^n - 1 - (A + B) \geq 2^n - 1$ so the sign bit is 1 and the result represents a negative number with magnitude $(A + B)$.

Unit 1 Solutions

1.44 Two positive numbers

No overflow: $0x\dots x + 0x\dots x = 0x\dots x$

carry in = 0 = carry out

Overflow: $0x\dots x + 0x\dots x = 1x\dots x$

carry in = 1, carry out = 0

Two negative numbers

No overflow: $1x\dots x + 1x\dots x = 1x\dots x$

carry in = 1 = carry out

Overflow: $1x\dots x + 1x\dots x = 0x\dots x$

carry in = 0, carry out = 1

A positive and a negative number

No overflow: $0x\dots x + 1x\dots x = 0x\dots x$

carry in = 1 = carry out

No overflow: $0x\dots x + 1x\dots x = 1x\dots x$

carry in = 0 = carry out

1.46 If $b_{n-1} = 0$, then $b_{n-2}2^{n-2} + b_{n-3}2^{n-3} + \dots + b_12 + b_0$ is the value of the positive number. If $b_{n-1} = 1$, then

$$-2^{n-1} + b_{n-2}2^{n-2} + b_{n-3}2^{n-3} + \dots + b_12 + b_0$$

$$= -(2^{n-2} + 2^{n-3} + \dots + 2 + 1 + 1) +$$

$$b_{n-2}2^{n-2} + b_{n-3}2^{n-3} + \dots + b_12 + b_0$$

$$= -[(1 - b_{n-2})2^{n-2} + (1 - b_{n-3})2^{n-3} + \dots + (1 - b_1)2 + (1 - b_0) + 1].$$

The expression in brackets has each bit complemented and 1 added to the result.

1.45

There is no overflow if the carry into the sign position equals the carry out of the sign position. There is overflow if the carry into the sign position does not equal the carry out of the sign position unless an end around carry causes a carry into the sign position.

No overflow

$$\begin{array}{r} 10101 \\ + 11010 \\ \hline (1)01111 \\ \xrightarrow{\quad} 1 \\ \hline 10000 \end{array}$$

Overflow

$$\begin{array}{r} 11001 \\ + 10101 \\ \hline (1)01110 \\ \xrightarrow{\quad} 1 \\ \hline 01111 \end{array}$$

Unit 1 Solutions